UNIST | SCHOOL OF ENERGY AND CHEMICAL ENGINEERING

Development of High Performance p-type Semiconductors for Transistors

- Time: 2025.12.02. (Tue) 16:00-17:15
- Place: 104-E206 Classroom

Speaker

Prof. Yong-Young Noh

Dept. of Chemical Engineering, POSTECH

Abstract

Developing high-mobility p-type semiconductors that can be grown using silicon-compatible processes at low temperatures, has remained challenging in the electronics community to integrate complementary electronics with the well-developed n-type counterparts.

This presentation will discuss our recent progress in developing high-performance p-type semiconductors as channel materials for thin film transistors. For the first part of my talk, I present an amorphous p-type oxide semiconductor composed of selenium-alloyed tellurium in a tellurium sub-oxide matrix, demonstrating its utility in high-performance, stable p-channel TFTs, and complementary circuits [1]. Theoretical analysis unveils a delocalized valence band from tellurium 5*p* bands with shallow acceptor states, enabling excess hole doping and transport. Selenium alloying suppresses hole concentrations and facilitates the *p* orbital connectivity, realizing high-performance p-channel TFTs with an average field-effect hole mobility of ~15 $cm^2\ V^{-1}\ s^{-1}$ and on/off current ratios of 10^6~10^7, along with wafer-scale uniformity and long-term stabilities under bias stress and ambient aging.

Next, I will present high-performance tin (Sn^{2+}) halide perovskite based p-type transistors using cesium-tin-triiodide-based semiconducting layers [2, 3]. The optimized devices exhibit high field-effect hole mobilities of over 50 $cm^2\ V^{-1}\ s^{-1}$, large current modulation greater than 10^8, and high operational stability and reproducibility [4]. In addition, we explore triple A-cations of caesium-formamidinium-phenethylammonium to create high-quality cascaded Sn perovskite channel films. As such, the optimized TFTs show record hole mobilities of over 70 $cm^2\ V^{-1}\ s^{-1}$ and on/off current ratios of over 10^8, comparable to the commercial low-temperature polysilicon technique level. In the final part, I would like to briefly introduce our recent halide perovskite transistors, fabricated by thermal evaporation [5].

References

[1] A. Liu, Y.-Y. Noh et al, Nature, **629**, 798–802 (2024)

[2] A. Liu, Y.-Y. Noh et al, Nature Electronics **5**, 78-83 (2022)

[3] H. Zhu, Y.-Y. Noh et al, Nature Electronics **6**, 650-657 (2023)

[4] A. Liu, Y.-Y. Noh et al, Nature Electronics **6**, 559-571 (2023)

[5] Y, Reo, Y.-Y. Noh et al, Nature Electronics, **8**, 403-410 (2025).